

**IN THE CLAIMS**

1-19. (Canceled)

20. (Currently Amended) A semiconductor integrated circuit device comprising:  
a plurality of internal circuits arranged internally in a circuit forming region, said internal circuits having different [~~difference~~] power lines;  
an inter-circuit signal wire arranged to interconnect said internal circuits; and  
an inter-circuit auxiliary wire connected to a static area near a location at which said inter-circuit signal wire is connected.

21. (Original) A semiconductor integrated circuit device according to claim 20, wherein each of said internal circuits includes a multiplicity of basic cells for active elements regularly arranged in repetition.

22. (Original) A semiconductor integrated circuit device according to claim 20, further comprising a substrate formed in a single chip, and said circuit forming region is allocated to one surface of said substrate.

23. (Original) A semiconductor integrated circuit device according to claim 22, wherein said circuit forming region includes signal input/output circuits outside said internal circuits, and external connection terminals outside said input/output circuits.

24. (Currently Amended) A semiconductor integrated circuit device according to claim 20, wherein said static area includes a partial region of an active element on a transmission side of said active elements in the first connection configuration connected to said inter-circuit signal wire, said partial region being connected to a power line of said internal circuit associated therewith, and an active element in a second [~~another~~] connection configuration having an identical or similar structure to said active element in the first connection configuration on a reception side, [and] said active element in the second connection configuration being arranged near said active element in the first connection configuration, [said active element in the other connection configuration] and being isolated from signal wires other than said inter-circuit auxiliary wire.

25. (Currently Amended) A semiconductor integrated circuit device according to claim 24, wherein a plurality of said active elements in the second [~~other~~] connection configuration are arranged to sandwich or surround said active element in the first connection configuration.

26. (Currently Amended) A semiconductor integrated circuit device according to claim 24, wherein each of said internal circuits includes a multiplicity of basic cells for active elements regularly arranged in repetition, and said active element in the first connection configuration and said active elements in the second [~~other~~] connection configuration are allocated to some of said basic cells.

27. (Original) A semiconductor integrated circuit device according to claim 24, further comprising a substrate formed in a single chip, and said circuit forming region is allocated to one surface of said substrate.

28. (Original) A semiconductor integrated circuit device according to claim 27, wherein said circuit forming region includes signal input/output circuits outside said internal circuits, and external connection terminals outside said input/output circuits.

29. (Original) A semiconductor integrated circuit device according to claim 24, wherein said inter-circuit auxiliary wire is connected to a neighboring region overlapping with or close to said partial region on said power line connected thereto, instead of said partial region.

30. (Currently Amended) A semiconductor integrated circuit device according to claim 24, wherein:

a plurality of said inter-circuit signal wires having different communication directions from each other are arranged to interconnect a [in any] pair of [said plurality of] internal circuits; an active element in a third [further] connection configuration having an identical or similar structure to said active element in the second [other] connection configuration is arranged in addition to said active element in the second [other] connection configuration near an active element in the first connection configuration on a reception side of said inter-circuit signal wire in one of said pair of internal circuits, said active element in the third [further] connection configuration being connected to a power line of said internal circuit and being isolated from said inter-circuit signal wire, other signal wires and said inter-circuit auxiliary wire; and

said active elements in the second [either] connection configuration are arranged independent [~~instead of or exclusive~~] of said active element in the third [further] connection configuration, near said active element in the first connection configuration on a reception side of said inter-circuit signal wire in the other one of said pair of internal circuits.

31. (Currently Amended) A semiconductor integrated circuit device according to claim 30, wherein [~~a group of elements including a plurality of either said active elements in the first connection configuration,~~] said active elements in the second [either] connection configuration[, or] and said active elements in the third [further] connection configuration are arranged to sandwich or surround said active element in the first connection configuration.

32. (Currently Amended) A semiconductor integrated circuit device according to claim 30, wherein each of said internal circuits includes a multiplicity of basic cells for active elements regularly arranged in repetition, and said active element in the first connection configuration, said active elements in the second [either] connection configuration, and said active elements in the third [further] connection configuration are allocated to some of said basic cells.

33. (Original) A semiconductor integrated circuit device according to claim 30, further comprising a substrate formed in a single chip, and said circuit forming region is allocated to one surface of said substrate.

34. (Original) A semiconductor integrated circuit device according to claim 33, wherein said circuit forming region includes signal input/output circuits outside said internal circuits, and external connection terminals outside said input/output circuits.

35. (Currently Amended) A semiconductor integrated circuit device according to claim 29, wherein:

a plurality of said inter-circuit signal wires having different communication directions from each other are arranged to interconnect a [in any] pair of [~~said plurality of~~] internal circuits; an active element in a further connection configuration having an identical or similar structure to said active element in the second [~~other~~] connection configuration is arranged in addition to said active element in the second [~~other~~] connection configuration near an active element in the first connection configuration on a reception side of said inter-circuit signal wire in one of said pair of internal circuits, said active element in the third [~~further~~] connection configuration being connected to a power line of said internal circuit and being isolated from said inter-circuit signal wire, other signal wires and said inter-circuit auxiliary wire; and said active elements in the second [~~other~~] connection configuration are arranged independent [~~instead of or exclusive~~] of said active element in the third [~~further~~] connection configuration, near said active element in the first connection configuration on a reception side of said inter-circuit signal wire in the other of said pair of internal circuits.

36. (Currently Amended) A semiconductor integrated circuit device according to claim 35, wherein [~~a group of elements including a plurality of either said active elements in the first connection configuration,~~] said active elements in the second [~~other~~] connection configuration[;

er] and said active elements in the third [further] connection configuration are arranged to sandwich or surround said active element in the first connection configuration.

37. (Currently Amended) A semiconductor integrated circuit device according to claim 35, wherein each of said internal circuits includes a multiplicity of basic cells for active elements regularly arranged in repetition, and said active element in the first connection configuration, said active elements in the second [ether] connection configuration, and said active elements in the third [further] connection configuration are allocated to some of said basic cells.

38. (Original) A semiconductor integrated circuit device according to claim 35, further comprising a substrate formed in a single chip, and said circuit forming region is allocated to one surface of said substrate.

39. (Original) A semiconductor integrated circuit device according to claim 38, wherein said circuit forming region includes signal input/output circuits outside said internal circuits, and external connection terminals outside said input/output circuits.

40. (Currently Amended) A semiconductor integrated circuit device comprising:  
a plurality of internal circuits arranged internally in a circuit forming region, said internal circuits having different [difference] power lines;  
a plurality of input/output circuits arranged outside said internal circuits;  
a plurality of external connection terminals outside said input/output circuits;

a signal wire passing through an input/output circuit belonging to [in] one of a plurality of sets each comprised of at least one [any of] said internal circuit [circuits] and at least one [any of] said input/output circuit, said plurality of sets each being connected to respective common power lines, said signal wire reaching an [said] internal circuit belonging to [included in] the same set as said input/output circuit through which said signal wire passes, said signal wire originating from one [any] of said external connection terminals;

a branched wire branched from said signal wire and passing through an [said] input/output circuit belonging to another one [in any other set] of said plurality of sets, and reaching an [said] internal circuit belonging to [in] the same set as said input/output circuit through which said branched wire passes;

a first protection circuit for said signal wire arranged in said input/output circuit of said one set [~~for said signal wire~~];

a second protection circuit for said branched wire arranged in said input/output circuit in said another set [~~for said branched wire~~]; and

a third protection circuit for said branched wire arranged in said internal circuit in said another [other] set [~~for said branched wire~~].

41. (Original) A semiconductor integrated circuit device according to claim 40, wherein each of said internal circuits includes a multiplicity of basic cells for active elements regularly arranged in repetition.

42. (Original) A semiconductor integrated circuit device according to claim 40, further comprising a substrate formed in a single chip, and said circuit forming region is allocated to one surface of said substrate.

43. (Original) A semiconductor integrated circuit device according to claim 40, wherein said third protection circuit includes a plurality of protection elements, said protection elements being arranged to sandwich or surround an element to be protected.

44. (Currently Amended) A semiconductor integrated circuit device according to claim 40, wherein at least one [either] of said first, second and [or] third protection circuits [circuit] includes an active element connected to a power line of an associated input/output [circuit] or [an associated] internal circuit, and isolated from any signal wire.

45. (Original) A semiconductor integrated circuit device according to claim 44, wherein said third protection circuit includes a plurality of protection elements, said protection elements being arranged to sandwich or surround an element to be protected.